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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No
BUR9-2000-0016-US1

Total Pages in this Submission
4

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

and invented by:

Ramachandra Divakaruni; Russell J. Houghton; Jack A. Mandelman; Wilbur D. Pricer; William R. Tonti

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 23 pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☐ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets **20 (Figs. 1-20B)**
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
    ☐ First Class ☒ Express Mail *(Specify Label No.):* **EL046033892US**

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

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Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	22	- 20 =	2	x	$18.00	$36.00
Indep. Claims	4	- 3 =	1	x	$80.00	$80.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$710.00
OTHER FEE *(specify purpose)* _____						$0.00
					TOTAL FILING FEE	$826 00

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☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of **$826.00** as filing fee.
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- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: 11/21/00

Eugene I. Shkurko, Esquire
Registration No.: 36,678
International Business Machines Corporation
Intellectual Property Law - Zip 972E
1000 River Street
Essex Junction, VT 05452

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Express Mail No.
EL046033892US

APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANTS: Ramachandra Divakaruni
Russell J. Houghton
Jack A. Mandelman
Wilbur D. Pricer
William R. Tonti

FOR: LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

DOCKET NO.: BUR9-2000-0016-US1

INTERNATIONAL BUSINESS MACHINES CORPORATION

LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to the formation of vertical bipolar transistors and more particularly to a method and process of forming vertical bipolar transistors simultaneously with field effect transistors using a damascene process.

Description of the Related Art

Silicon-On-Insulator (SOI) technology, which is becoming of increasing importance in the field of integrated circuits, deals with the formation of transistors in a relatively thin layer of semiconductor material overlying a layer of insulating material. Devices formed on SOI offer many advantages over their bulk counterparts, including: higher performance, absence of latch-up, higher packing density, low voltage applications, etc. SOI technology provides a very high performance regime for complementary metal oxide semiconductor (CMOS)

operation due to a unique isolation structure.

It is advantageous in semiconductor manufacturing to simultaneously produce as many different types of devices on a chip has possible. Such simultaneous production reduces the number of steps and the amount of material required to make the chip. This reduces the time and cost of producing semiconductor chips. Therefore, it is desirable to simultaneously form different types of transistors on a single chip.

There is a conventional need to integrate a complementary pair of bipolar devices within the SOI CMOS framework for low voltage, high performance operation, thereby making use of as much of the SOI CMOS advantages as possible. The invention discussed below is directed to a methodology that simultaneously forms field effect transistors (e.g. CMOS transistors) and bipolar transistors using a damascene process to form the CMOS gates and the bipolar emitters.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method of forming an emitter in a vertical bipolar transistor. The emitter forms a patterned mask over the collector layer and fills openings in the mask with emitter material in a damascene process. The substrate includes an insulator layer

between a bottom silicon layer and a top silicon layer, and the invention implants a first impurity to form the collector layer in a lower portion of the top silicon layer adjacent the insulator layer, and a second impurity to form the base layer in an upper portion of the top silicon layer.

The emitter material includes a first impurity that is annealed to drive the first impurity into the base to create an emitter diffusion region in the base below each emitter. The substrate also includes a patterned second mask over the bipolar region, the mask includes openings through to the base layer between adjacent ones of the emitters, and the invention implants additional amounts of the second impurity into the base layer through the openings. The invention can also include forming a protective layer over the emitters and implanting additional amounts of the first impurity into the insulator layer to provide a collector contact diffusion region.

The invention also includes a method of simultaneously forming complementary methal oxide semiconductor devices and vertical bipolar transistors on an integrated circuit chip that includes providing a silicon over insulator substrate having a collector layer and a base layer over the collector; forming a polysilicon layer over a CMOS region of the SOI substrate, patterning a mask over the polysilicon layer and a bipolar region of the SOI substrate (the mask include openings over the bipolar region), depositing an emitter material in the openings in a damascene process to form emitters, removing the mask,

patterning the polysilicon layer to form gate conductors, and forming sidewall spacers adjacent the emitters and the gate conductors.

The invention also includes a CMOS/vertical bipolar structure, in which the collector, base regions, and emitter regions are vertically disposed on one another, the collector region having a peak dopant concentration adjacent the inter-substrate isolation oxide.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of preferred embodiments of the invention with reference to the drawings, in which:

Figure 1 is a cross-sectional schematic view of a stage of production of a bipolar transistor;

Figure 2 is a cross-sectional schematic view of a stage of production of a bipolar transistor;

Figure 3 is a cross-sectional schematic view of a stage of production of a CMOS transistor and a bipolar transistor;

Figure 4 is a cross-sectional schematic view of a stage of production of a CMOS transistor and a bipolar transistor;

Figure 5 is a cross-sectional schematic view of a stage of production of a

CMOS transistor and a bipolar transistor;

Figure 6 is a cross-sectional schematic view of a stage of production of a bipolar transistor;

Figure 7 is a cross-sectional schematic view of a stage of production of a bipolar transistor;

Figure 8 is a cross-sectional schematic view of a completed bipolar transistor;

Figure 9 is a perspective schematic view of bipolar transistors;

Figures 10A and 10B are graphs illustrating advantages produced by the invention;

Figure 11 is a cross-sectional schematic view of a stage of production of a bipolar transistor;

Figure 12 is a cross-sectional schematic view of a stage of production of a CMOS transistor and a bipolar transistor;

Figure 13 is a cross-sectional schematic view of a stage of production of a CMOS transistor and a bipolar transistor;

Figure 14 is a cross-sectional schematic view of a stage of production of a CMOS transistor and a bipolar transistor;

Figure 15 is a cross-sectional schematic view of a stage of production of a CMOS transistor and a bipolar transistor;

Figure 16 is a cross-sectional schematic view of a stage of production of a

bipolar transistor;

Figure 17 is a cross-sectional schematic view of a stage of production of a bipolar transistor;

Figure 18 is a cross-sectional schematic view of a completed bipolar transistor;

Figure 19 is a perspective schematic view of bipolar transistors; and

Figures 20A and 20B are graphs illustrating advantages produced by the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

The invention takes advantage of SOI technology and simultaneously forms CMOS transistors and bipolar transistors utilizing a damascene process. More specifically, as shown in Figure 1, the inventive process begins with a standard SOI structure. The structure includes a silicon substrate 10 (e.g. a bulk silicon) over which an insulator 12 (e.g., oxide layer) has been formed. A top silicon layer 15 is formed over the insulator 12.

The collector 14 (N + collector) is formed through an implant process as represented by arrows 19. Antimony has been found to be a suitable N-type impurity because of its relatively low disffusivity and small implant straggle

which enables the collector layer 14 to be confined near the back interface of the top silicon layer 15. Similarly, the P-type base 16 is formed by implants 19. Figure 1 also illustrates a screen oxide 18 (such as a MOSFET screen oxide) is formed over the structure.

In one preferred embodiment, the SOI layer 10, 12, 15 could have a thickness of approximately 400nm. The collector 14 implant 19 preferably has a dose of 1 x 1016cm^{-2} at a power of 1MeV. This doping profile (and other similar doping profiles that would be known by those ordinarily skilled in the art given this disclosure) produces a buried collector 14 centered at approximately the back interface of the silicon 15 and insulate or 12 layers with a peak concentration of approximately 3 x 10^{19}cm^{-3}.

Having the collector 14 and base 16 profiles vertically stacked results in an extremely narrow base width (Wb in Figure 8), and a collector junction which terminates on the back oxide 12 of the SOI layer, meeting the device design objectives for high performance. The collector terminating on the back oxide reduces collector capacitance, thereby improving bipolar transistor performance. Further, the collector 14 and the base 16 are implanted with the same mask. This mask also protects the CMOS area of the wafer from receiving either implant.

In Figure 2, a thick nitride layer 20 is deposited over the bipolar and CMOS regions. The nitride is subsequently etched over the CMOS regions. The nitride layer 20 limits the gate oxidation to the CMOS regions. As shown below,

the nitride layer 20 is used to damascene a bipolar emitter. The thickness of this nitride 20 is: $T_{(N2)} = T_{(GC)} - \Delta T_{(polish)}$ where: $T_{(n2)}$ is the thickness of the nitride deposited and is equal to the final desired gate conductor (GC) thickness (in the CMOS devices) minus a delta "physical" polish stop support nitride thickness (to be later deposited over the entire wafer to eliminate over-polish of GC only regions i.e., the CMOS region). $T_{(GC)}$ is the final desired GC thickness and $\Delta T_{(polish)}$ is the second nitride thickness required to form a polish stopping layer.

A photoresist mask (not shown) is used over the bipolar region to protect it from the CMOS device well implants. This mask is not additional, but rather it is simply a different mask having alternate blocking levels used to differentiate N-Well from P-Well areas. Therefore, the bipolar devices are protected from the CMOS device well implants without increasing the processing steps associated with standard processing.

Figure 3 illustrates a CMOS device on the left side and a bipolar device on the right side as both would be simultaneously formed on a single wafer using the invention. The CMOS region includes the same SOI structure 10, 12, 15. In addition, a gate oxide 32 is formed within the CMOS region. The gate oxide 32 is not formed in the bipolar region by operation of the nitride mask 20. In Figure 3 an intrinsic polysilicon 30 is formed over both structures.

Figure 4 illustrates the formation of the bipolar transistor emitters 42.

More specifically, the polysilicon 30 is removed from the bipolar region utilizing a mask or other protective structure to allow for the intrinsic polysilicon 30 to remain in the CMOS region. An additional nitride layer 40 is deposited over the entire wafer. Subsequently, openings are patterned through the nitride layers 40, 20 in the bipolar region and the openings are filled in a damascene process with an N+ doped polysilicon to form N+ polysilicon emitters 42. Then, the structure is polished to remove the nitride 40.

As shown in Figure 5, the nitride 20, 40 is removed. In a separate processing step, the polysilicon 30 remaining over the CMOS region is patterned into gates 30. The bipolar devices are protected by a mask during the patterning of the gates 30. Subsequently, sidewall spacers 50 are simultaneously formed over the gates 30 and the emitters 42, using any of a number of well-known sidewall spacer formation technologies.

Next, in Figure 6, a block mask 62 is formed over the emitters 42. This same mask protects PFET devices and exposes NFET junctions (not shown). An N+ implant is then performed to provide the N+ collector contact implant 60 and simultaneously dopes the source/drain structures of the NFETs (not shown).

Openings 70 are patterned in the block mask 62 to allow the P+ diffusion implant 72 in the base 16, as shown in Figure 7. In one embodiment, the P+ implant is a low energy high dose p-type implant. Such an implant would preferably be simultaneously performed with either a contact or extension implant

in the parallel CMOS process. Alternatively, the P+ implant may be performed using an extra mask and implant if the particular SOI CMOS process does not utilize a similar contact or extension implant. The invention avoids using the PFET P+ junction implant in the CMOS process for the diffusion implant 72, as the P+ junction CMOS implant may reach through to the collector and destroy the functionality of the bipolar transistor.

The block mask 62 is removed, as shown in Figure 8. An annealing process drives the N+ 60, P+ 72 and emitter N+ 80 (from the N+ polysilicon 42) impurities into place, as shown in Figure 8.

In Figures 8 and 9 the completed bipolar transistor is shown in cross section and perspective views as it might appear in a typical layout using multiple emitters 42. Contacts to the CMOS device and the vertical bipolar transistor are formed to this structure using conventional methods well known to those ordinarily skilled in the art. Such connections are not shown to not unnecessarily obscure the invention.

The collector doping profile and the D.C. performance of the device is shown in Figures 10A and 10B. The flat part of the collector doping profile shown in Fig. 10A lies in the interior of the collector region, which is adjacent to the back interface of the SOI layer. This plot shows the electrically active (as opposed to the chemical concentration) of the implanted antimony. The flat part of the profile in Figure 10A is attributed to the low solid solubility of antimony in

silicon and clustering effects.

The common emitter current gain (BETA, β) of the bipolar transistor, defined as $\Delta I_c/\Delta I_b$, is shown in Figure 10B. The current gain decreases with increasing base-emitter voltage (vbe) due to effects resulting from the flooding of the base with carriers.

Figures 10A and 10B indicate the viability of a high performance bipolar device fabricated within the constraints of SOI processing. Figures 10A and 10B also show that the invention allows the base width Wb to be selectively controlled by either growing/depositing selective silicon over the top surface of the SOI layer.

Figures 11-20 illustrate a second embodiment of the invention. This embodiment is similar to the previous embodiment; However in this embodiment the gate conductors and the emitters are formed using damascene processes. The invention produces an integrated damascene (CMOS/ bipolar process) reflecting all the advantages of damascene gate CMOS known in the art (i.e., the ability to provide channel doping away from source/drain which produces reduced junction capacitance, improved reliability). Therefore, the damascene emitter formation according to the invention represents a substantial improvement over existing technology.

Structures which are similar to those discussed above with respect to

Figures 1-9 are identified with the same numbers in Figures 11-19 and a redundant discussion of the same is omitted for the sake of brevity. Figure 11 is substantially similar to Figure 1 and illustrates base and collector implants 19 being made to an SOI structure 10, 12, 15. In Figure 12, a thick nitride layer 120 is deposited over the entire wafer. Then, in Figure 13, openings for the emitters are formed in the bipolar region and the emitter conductors 42 (again, an N+ polysilicon) are deposited in a damascene process.

In Figure 14, the gate conductors are formed by patterning openings through the thick nitride 120 in the CMOS region. Then, a gate oxide 140 is grown in the opening. Note that the gate oxide also forms over the emitters 42. Subsequently, the gate conductor 142 is formed in the remainder of the opening above the gate oxide 140. Note that the gate conductor 142 does not include a concentration of N+ doping (the gate poly is intrinsic) that the emitters 42 include. The N+ doping within the emitters 42 allows the emitter junction impurity 144 to be driven into the base 16 during subsequent annealing operations (which starts during the gate oxide 140 growth process).

Figure 15 illustrates formation of the spacers 50, as discussed above with respect to Figure 5. Similarly, Figure 16 illustrates the formation of the block mask 62 and the collector contact diffusion 60 in a similar process to that discussed above with respect to Figure 6. In Figure 17, openings 70 are again formed in the block mask 62 and the base diffusion implant is performed, in a

process similar to that discussed above with respect to Figure 7. In a similar manner to that discussed above with respect to Figures 8 and 9, Figures 18 and 19 illustrate the activation of the N+, P+ and emitter drive-in anneals 60, 72, 80.

Figures 20A-20B illustrate the performance achieved through this embodiment of the invention.

As discussed above, the invention includes fabrication sequences for a vertical SOI bipolar transistor, which is integrated into a typical logic process sequence. An NPN sequence is illustrated, but as would be known by one ordinarily skilled in the art given this disclosure, the invention can be easily modified to accommodate a PNP , thus offering a complementary pair.

In drawing a parallel to a CMOS fully depleted body, the inventive bipolar device is orientated vertically (see Figure 8) in SOI and has a base width Wb which is independent of the SOI thickness, and hence is very narrow. Since the charge of excess minority carriers in the base (ΔQ) is proportional to the base width Wb, and the base transit time, τb is proportional to ΔQ, the SOI effect on bipolar performance is scaled with the CMOS improvement.

Another improvement in bipolar performance arises from the reduced collector to substrate capacitance achieved with the invention as compared to a pure silicon vertical structure. In SOI CMOS, the P/N junction area capacitance term is negligible as the junction terminates on the back oxide. The vertical NPN

structure shown in Figure 8 takes advantage of this same design improvement for bipolar devices.

Applications for the inventive technology cover the spectrum from pure digital applications such as DRAM, eDRAM, SRAM, MRs to mixed-mode combined RF/digital applications such as communications products. This technology enables the concurrent use of high-performance CMOS digital logic and high-performance bipolar analog small signal circuitry on the same chip.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A method of forming an emitter in a vertical bipolar transistor comprising:

providing a substrate having a collector layer and a base layer over said collector layer;

forming a patterned mask over said collector layer; and

filling openings in said mask with emitter material in a damascene process.

2. The method in claim 1, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

3. The method in claim 2, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

4. The method in claim 2, further comprising:

patterning a second mask over said bipolar region, said mask including openings through to said base layer between adjacent ones of said emitters; and

implanting additional amounts of said second impurity into said base layer through said openings.

5. The method in claim 2, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into said insulator layer to provide a collector contact diffusion region.

6. A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

forming a polysilicon layer over a CMOS region of said SOI substrate;

patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region

depositing an emitter material in said openings in a damascene process to form emitters;

removing said mask;

patterning said polysilicon layer to form gate conductors; and

forming sidewall spacers adjacent said emitters and said gate conductors.

7. The method in claim 6, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

8. The method in claim 7, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

9. The method in claim 7, further comprising:

patterning a second mask over said bipolar region, said mask including second openings through to said base layer between adjacent ones of said emitters; and

implanting additional amounts of said second impurity into said base layer through said openings.

10. The method in claim 7, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into said insulator layer to provide a collector contact diffusion region.

11. The method in claim 6, further comprising, before said forming of said polysilicon, forming a gate oxide layer over said CMOS region of said SOI substrate.

12. A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer

and a base layer over said collector;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

13. The method in claim 12, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

14. The method in claim 13, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

15. The method in claim 13, further comprising:

patterning a second mask over said bipolar region, said mask including third openings through to said base layer between adjacent ones of said emitters; and

implanting additional amounts of said second impurity into said base layer through said third openings.

16. The method in claim 13, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into said insulator layer to provide a collector contact diffusion region.

17. The method in claim 12, further comprising, before said forming of said polysilicon, forming a gate oxide layer over said CMOS region of said SOI substrate.

18. A semiconductor structure including both a CMOS transistor and a vertical bipolar transistor, comprising:

a substrate having a lower semiconductor portion, an upper semiconductor portion, and an first insulator structure between said upper and lower semiconductor portions;

a collector region disposed in the upper semiconductor portion, said collector region having a peak dopant concentration adjacent the first insulator structure;

a plurality of base regions disposed in the upper semiconductor portion above the collector region;

a plurality of emitter diffusion regions disposed in the upper semiconductor portion, each abutting a respective one of the plurality of base regions;

a second insulator structure disposed on first selected portions of the upper semiconductor portion;

a plurality of first electrodes disposed on the upper semiconductor portion, each of the plurality of first electrodes forming an electrical contact to a respective one of the plurality of emitter diffusion regions; and

a second electrode formed on the second insulator structure, the second electrode comprising a gate electrode of the CMOS transistor.

19. The structure in claim 18, wherein the plurality of base regions and the plurality of emitter diffusion regions are surrounded by the collector region.

20. The structure in claim 19, further comprising a plurality of oxide isolation regions that abut the collector region.

21. The structure in Claim 18, wherein both of said plurality of first electrodes and said second electrode are comprised of a common polysilicon layer.

22. The structure of Claim 19, wherein the collector region extends substantially to an upper surface of the upper semiconductor portion.

LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

ABSTRACT

A method and structure for forming an emitter in a vertical bipolar transistor includes providing a substrate having a collector layer and a base layer over the collector layer, forming a patterning mask over the collector layer,, and filling openings in the mask with emitter material in a damascene process. The CMOS/vertical bipolar structure has the collector, base regions, and emitter regions vertically disposed on one another, the collector region having a peak dopant concentration adjacent the inter-substrate isolation oxide.

Figure 1

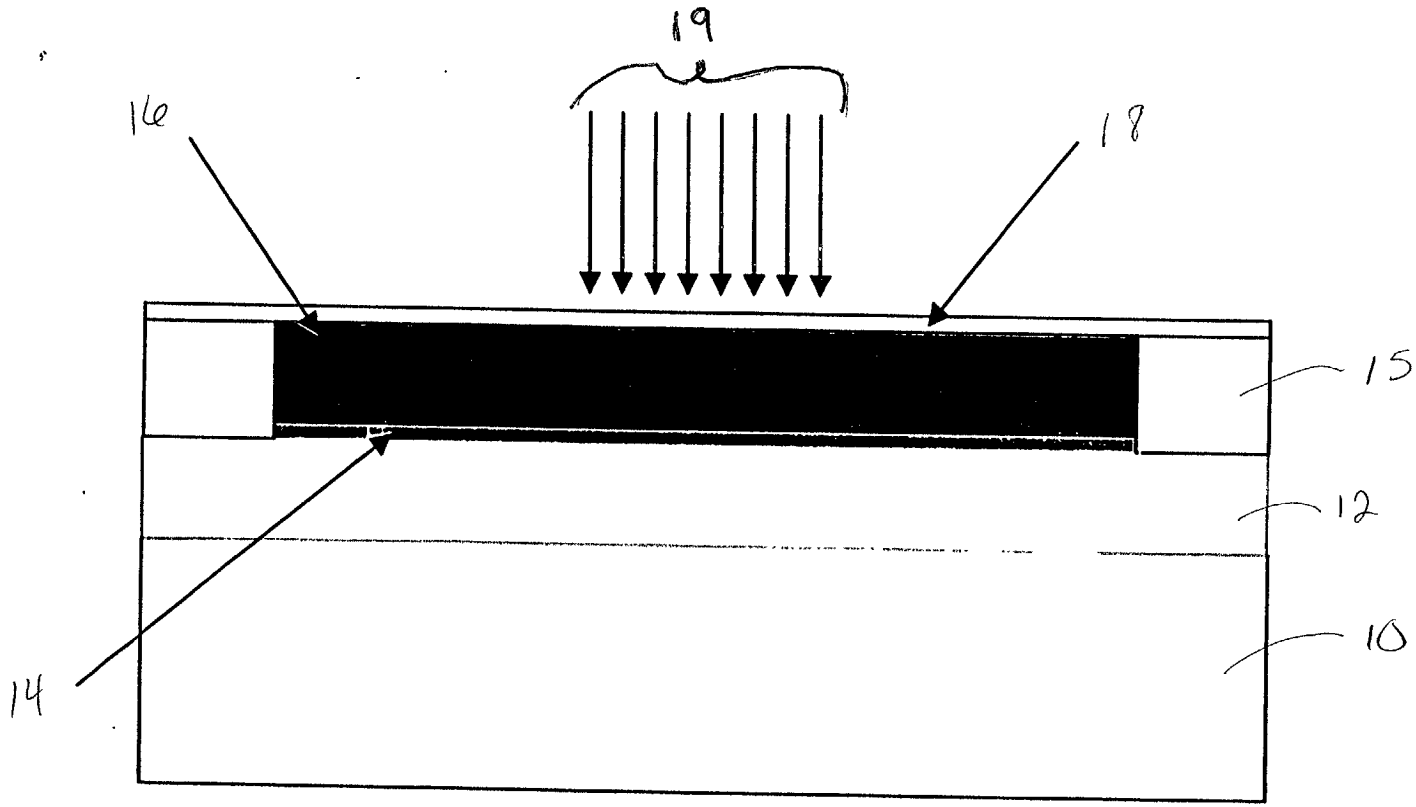

Figure 2

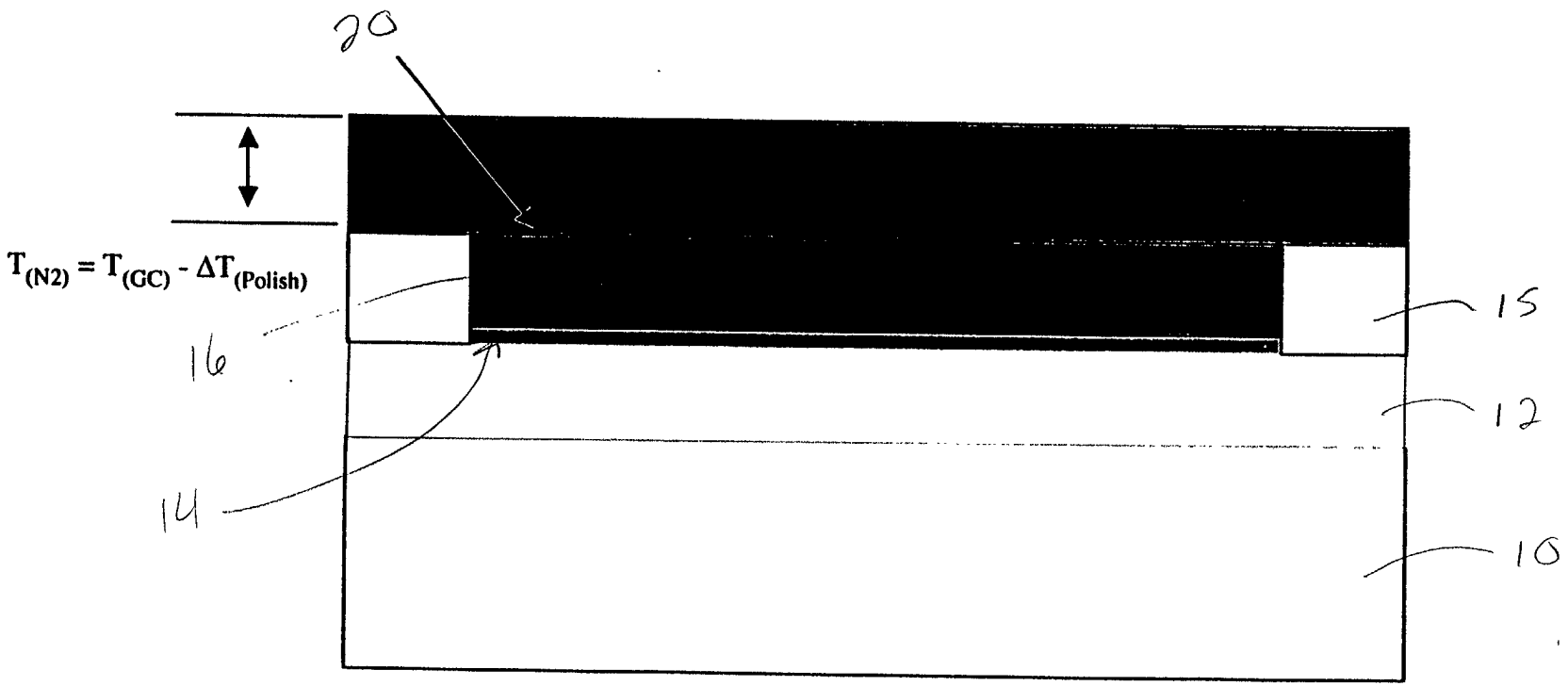

Figure 3

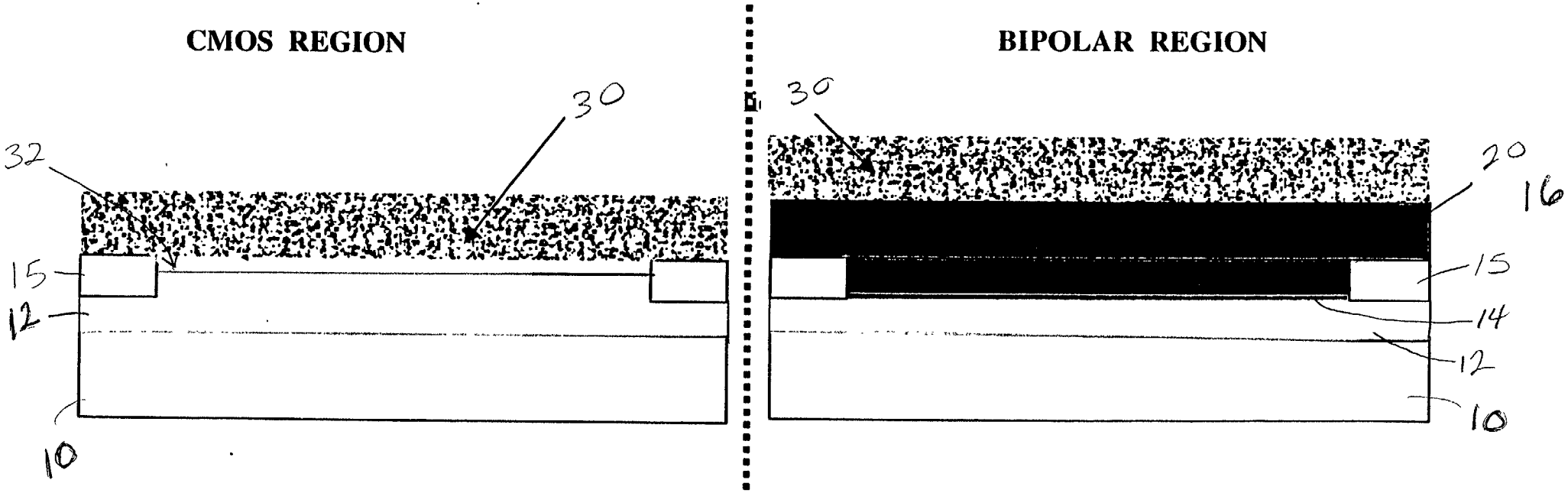

Figure 4

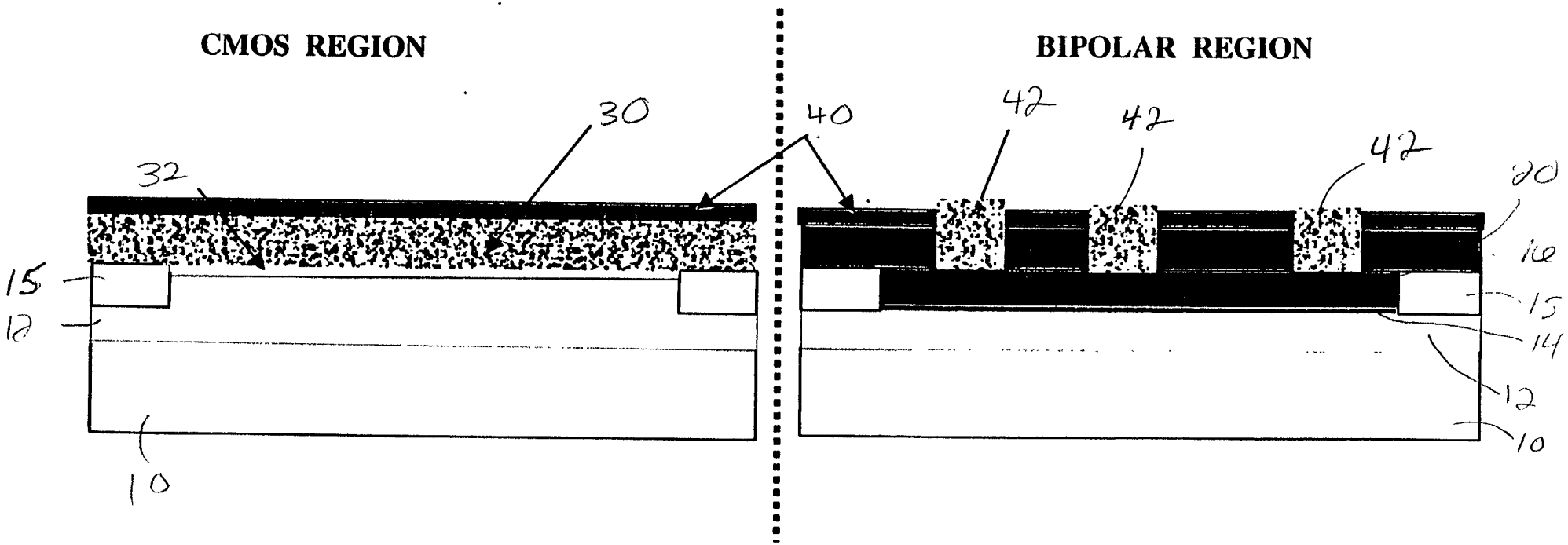
CMOS REGION
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Figure 5

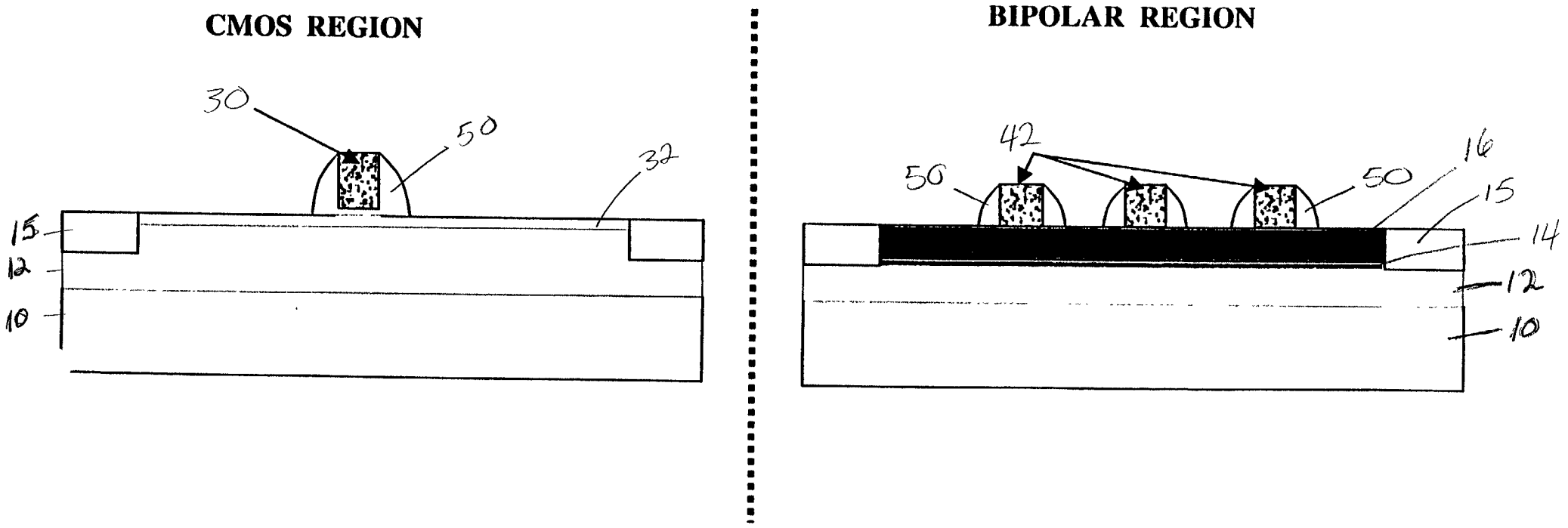

CMOS REGION
BIPOLAR REGION
30
50
32
15
12
10
42
50
50
16
15
14
12
10

Figure 6

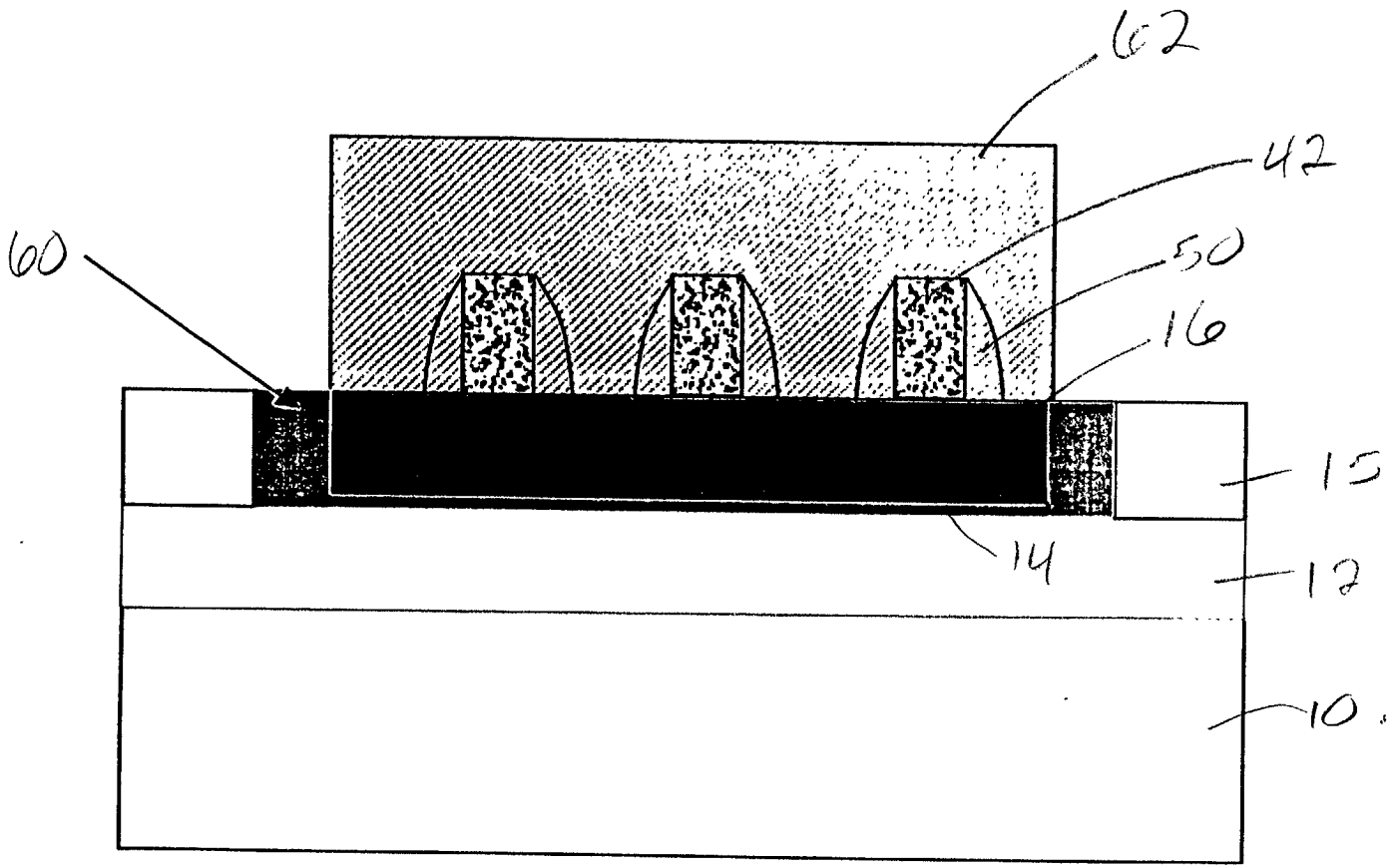


Figure 7

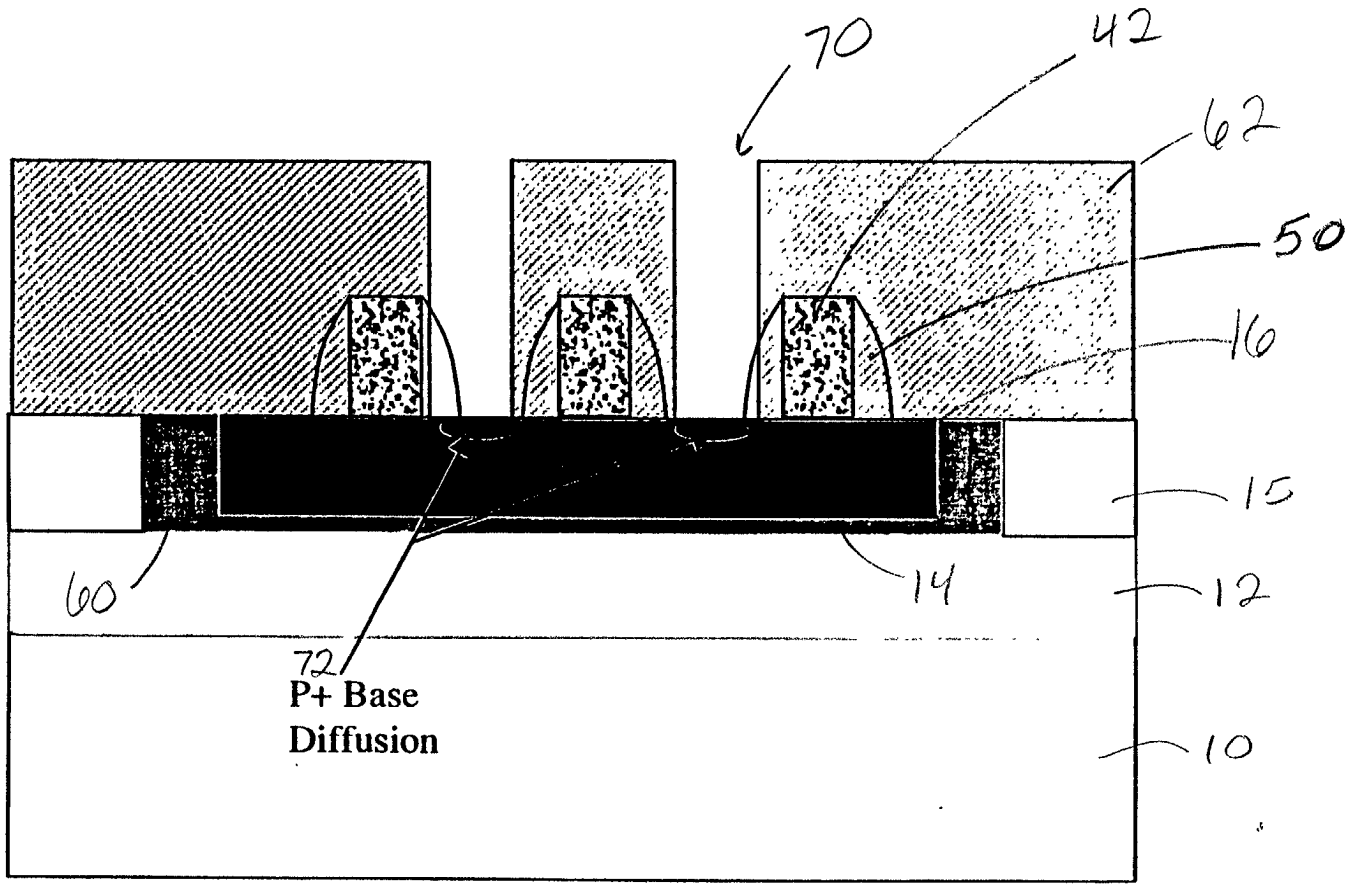


Figure 8

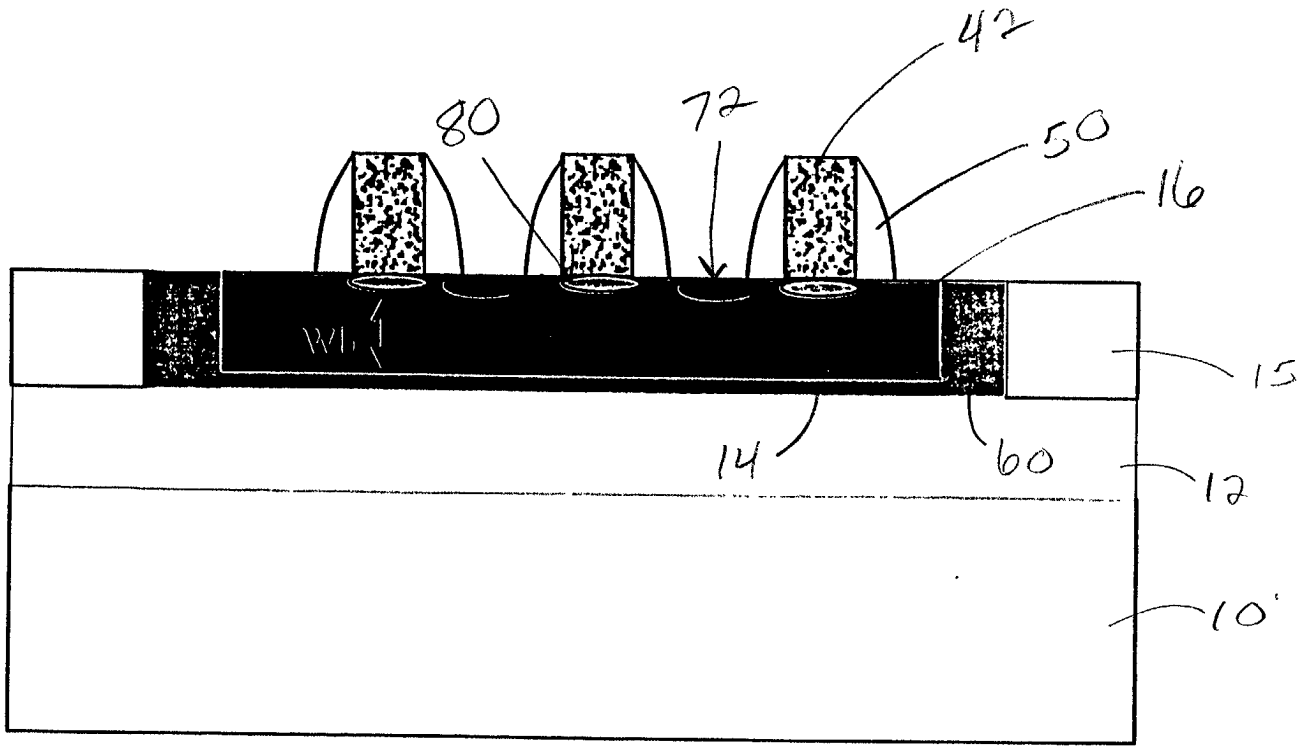
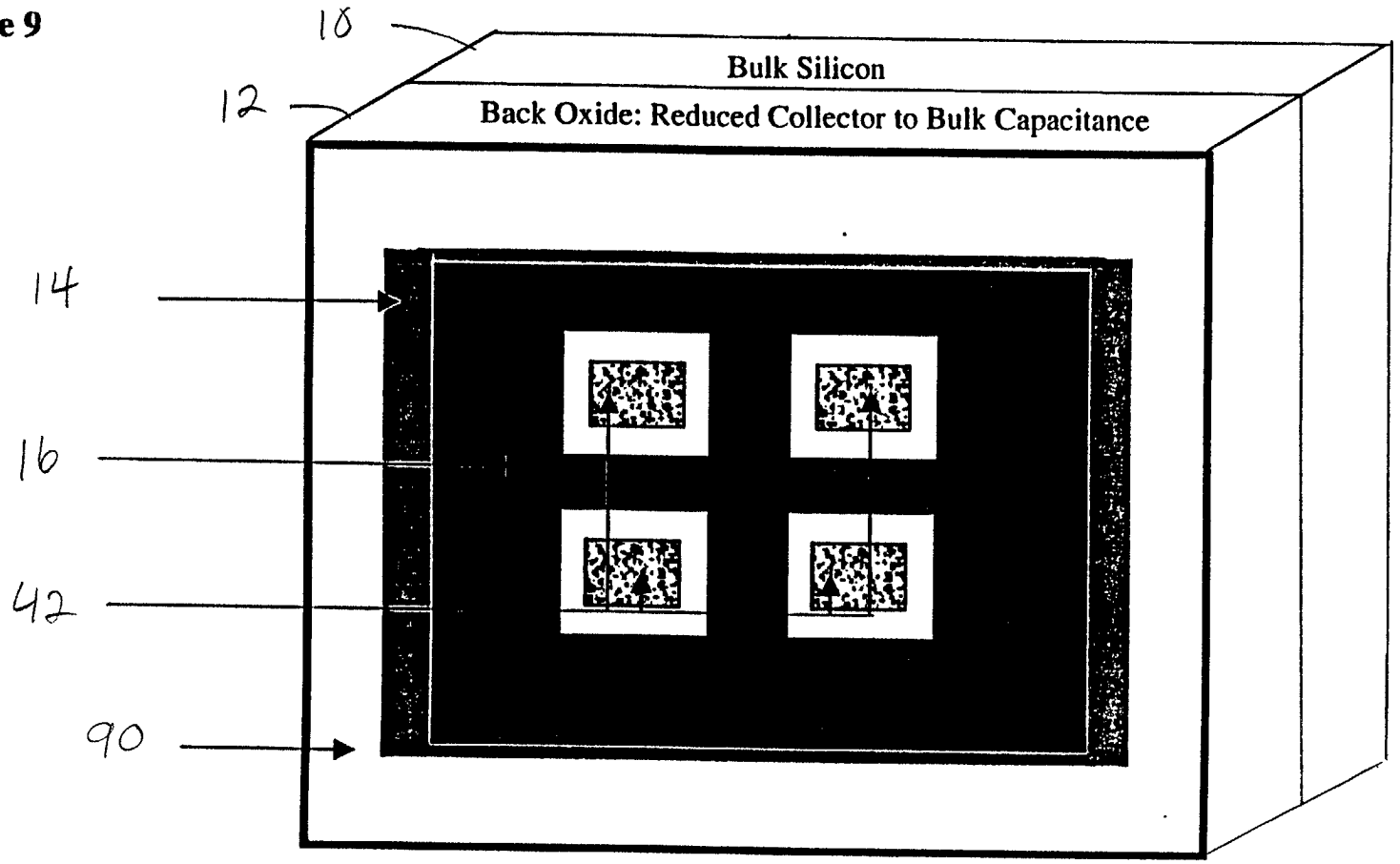


Figure 9


10
12
Bulk Silicon
Back Oxide: Reduced Collector to Bulk Capacitance
14
16
42
90

Collector Doping Profile

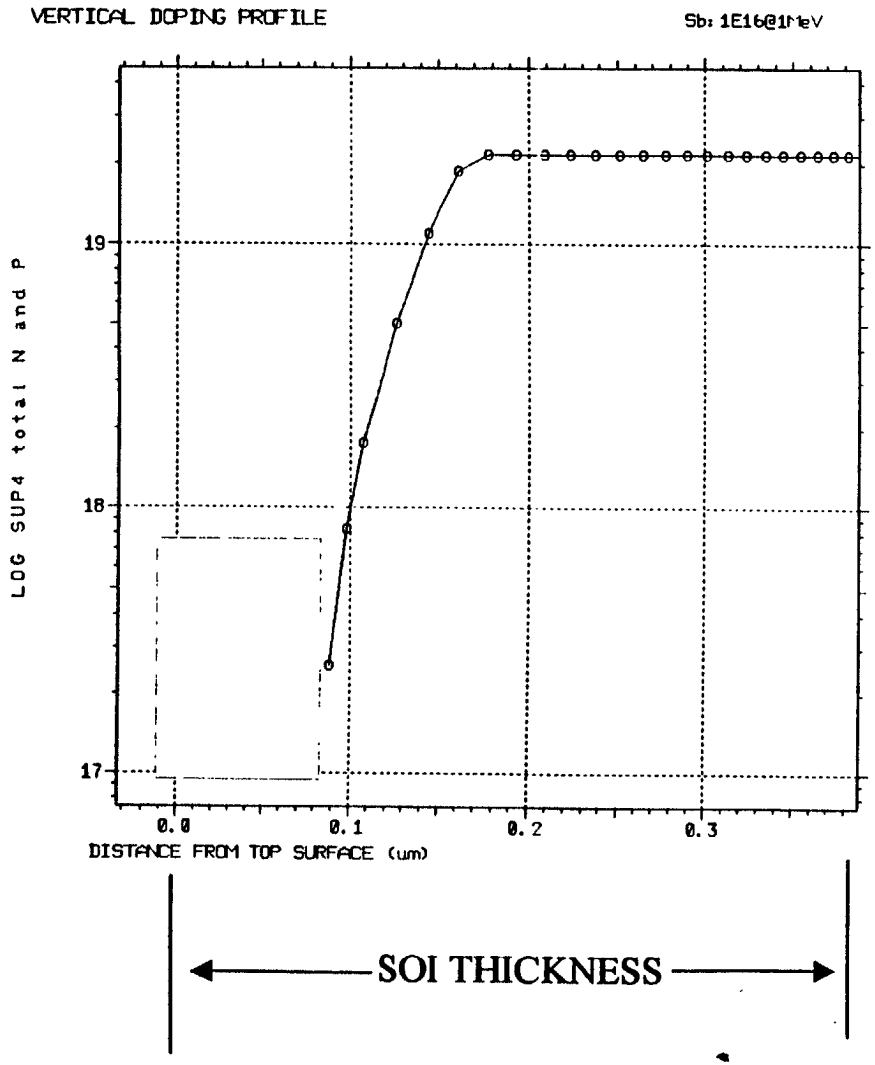


Figure 16A

D.C. Beta vs. Vbe

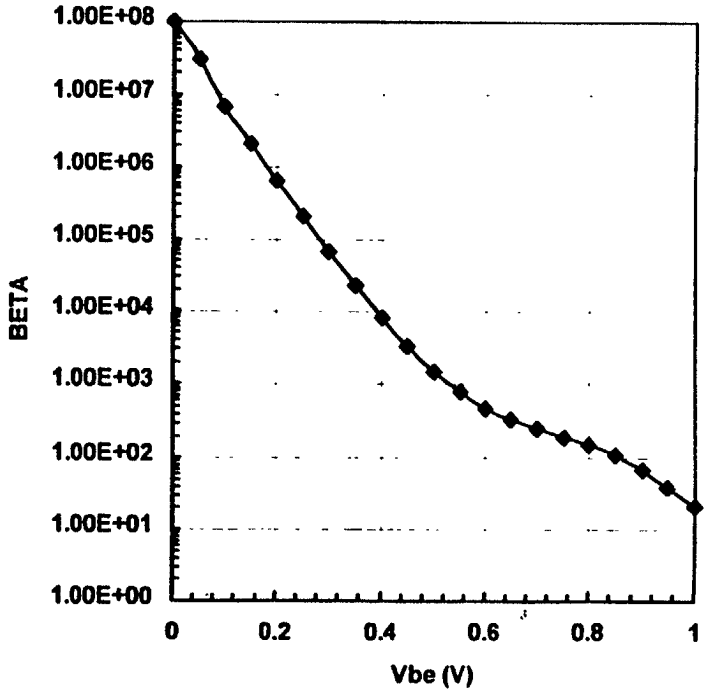


Figure 16B

Figure 11

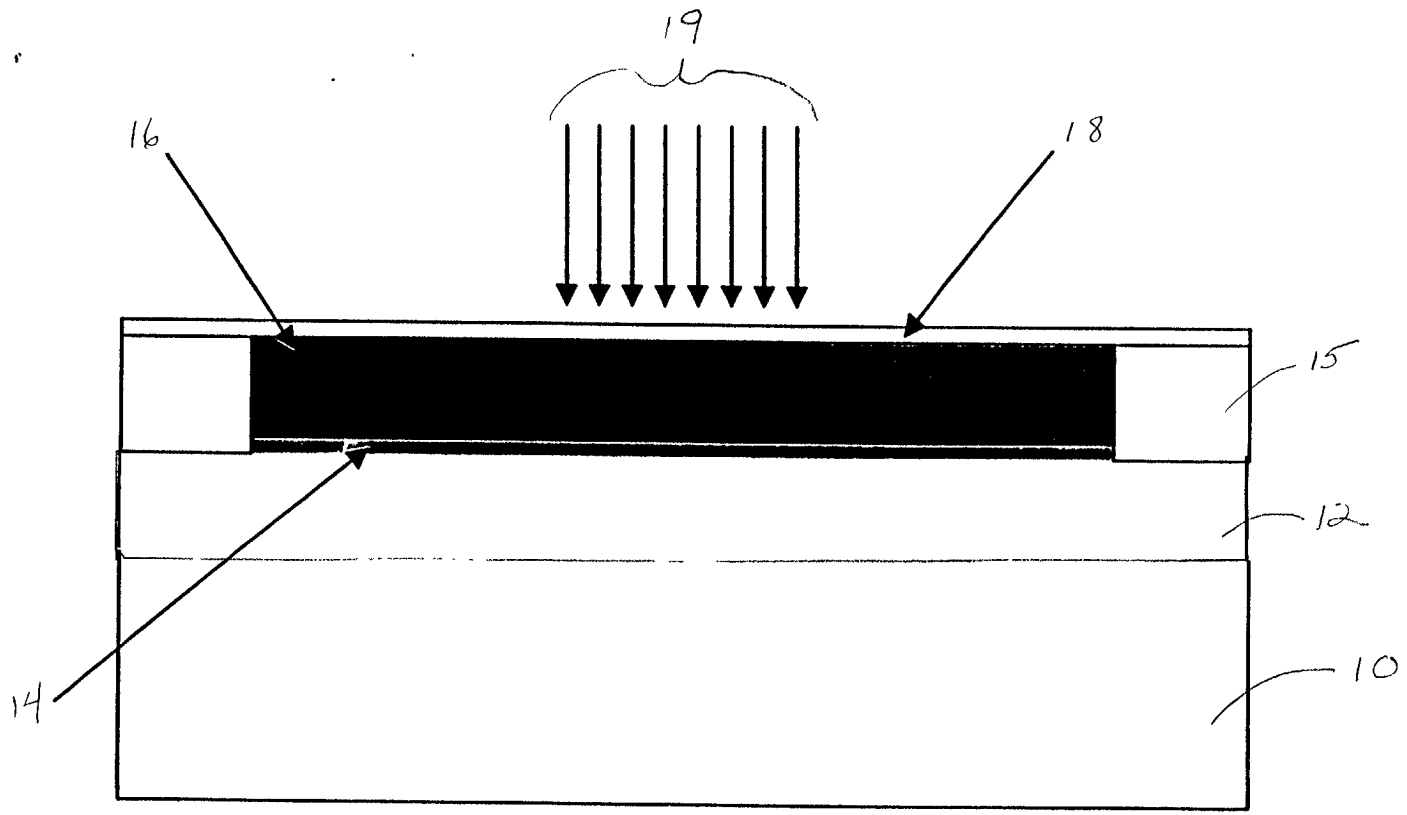


Figure 12

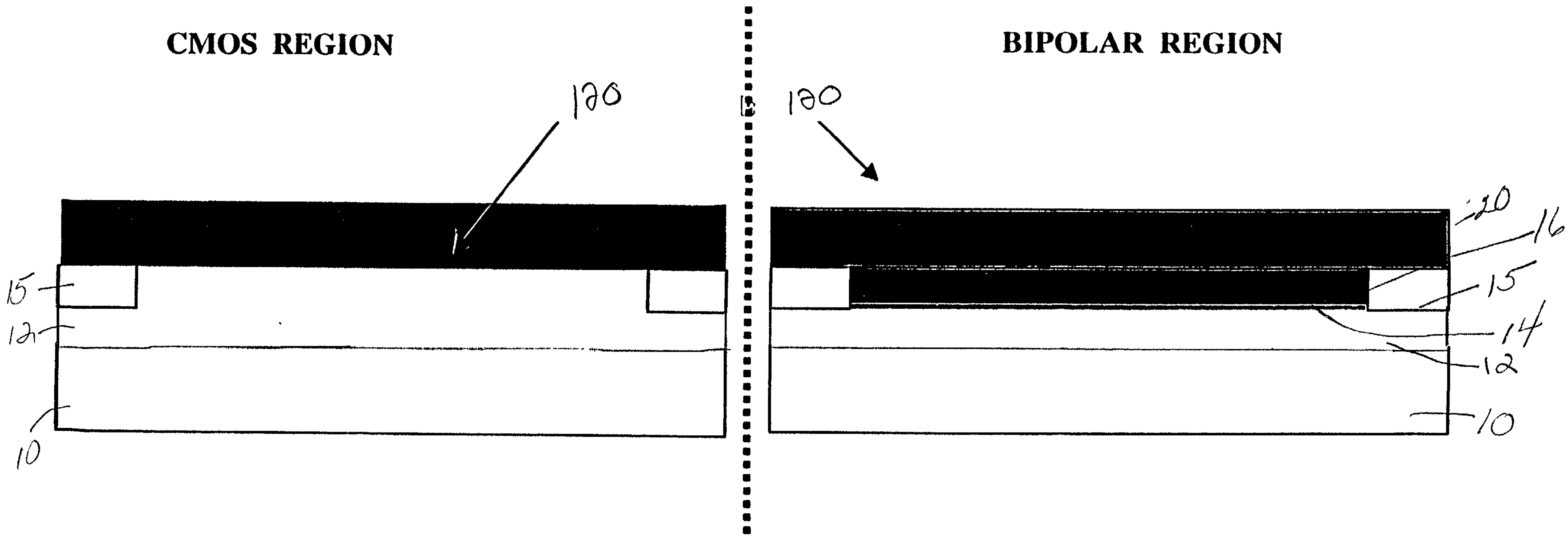


Figure 13

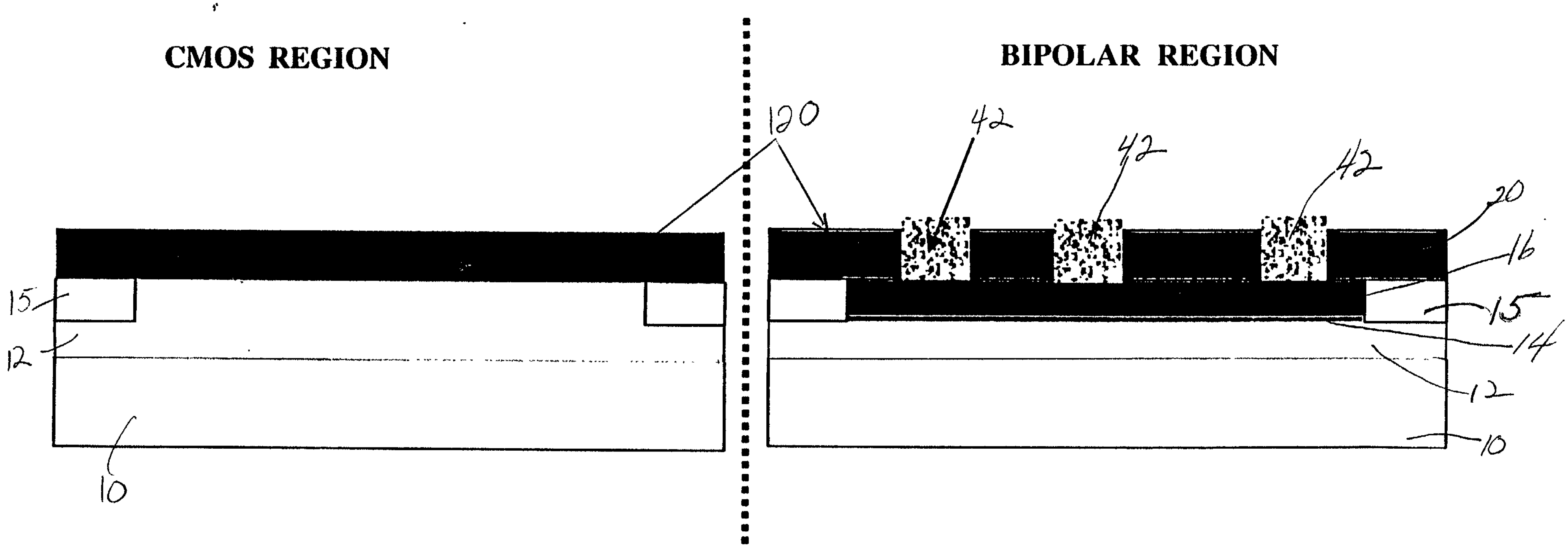

CMOS REGION
BIPOLAR REGION
120
42
42
42
20
16
15
14
12
10
15
12
10

Figure 14

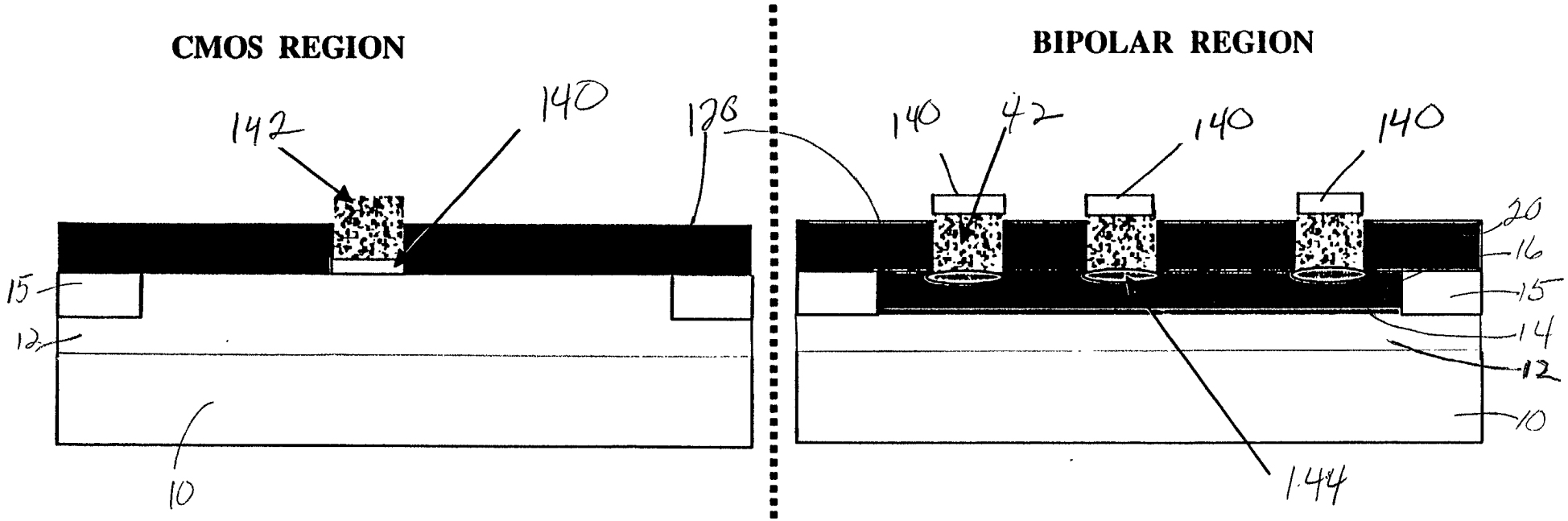

CMOS REGION
BIPOLAR REGION
142
140
128
140
42
140
140
20
16
15
14
12
10
15
12
10
144

Figure 15:

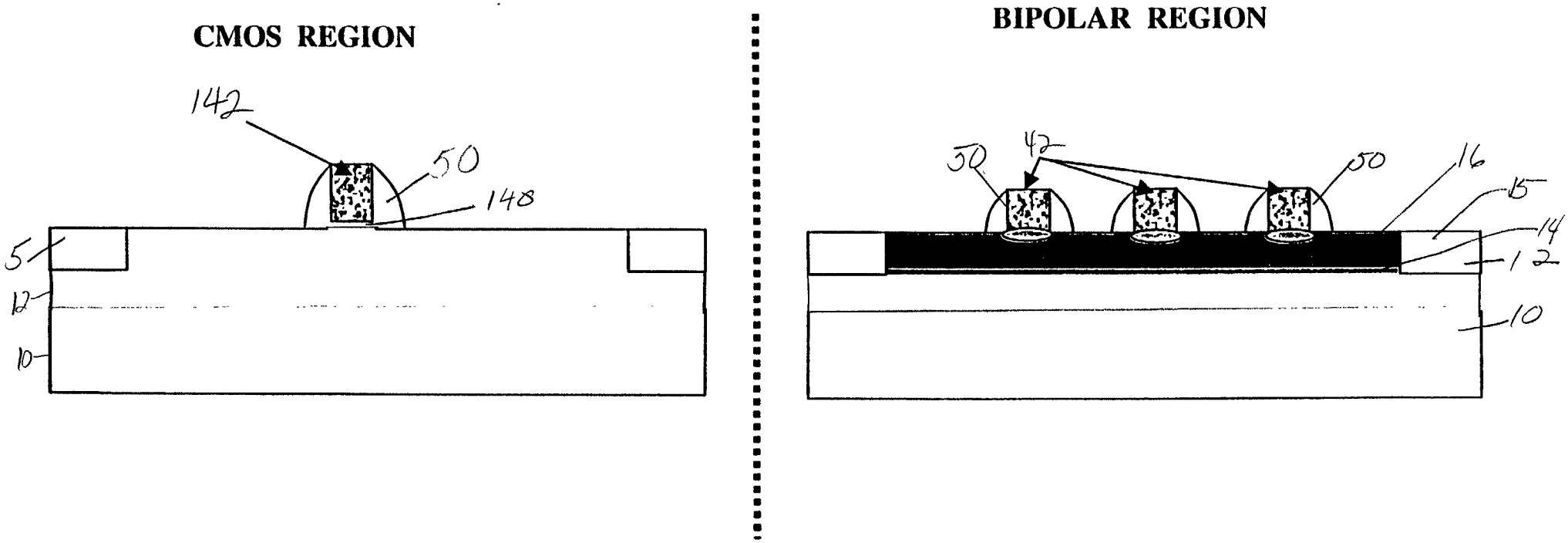

CMOS REGION
142
50
148
5
12
10
BIPOLAR REGION
50
42
50
16
15
14
12
10

Figure 16

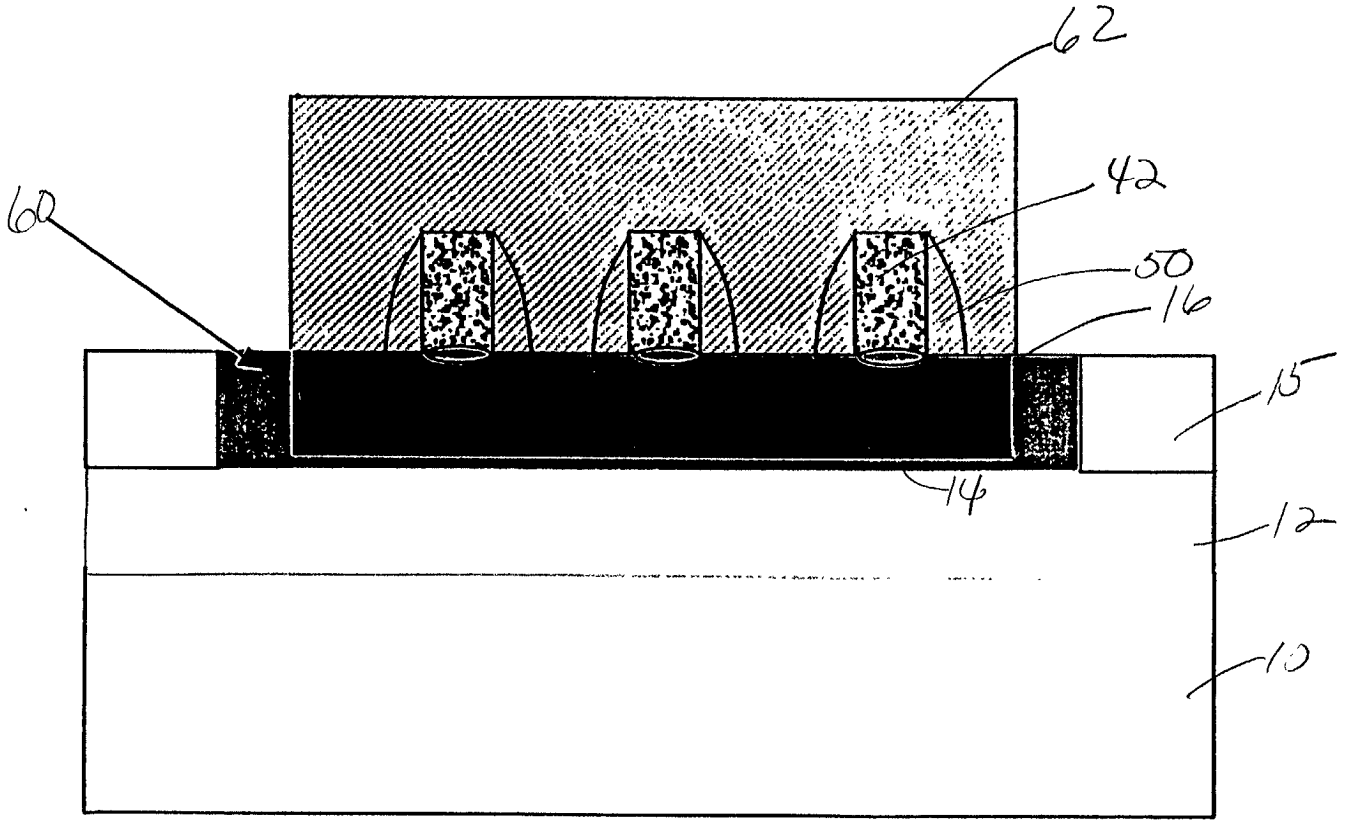


Figure 17

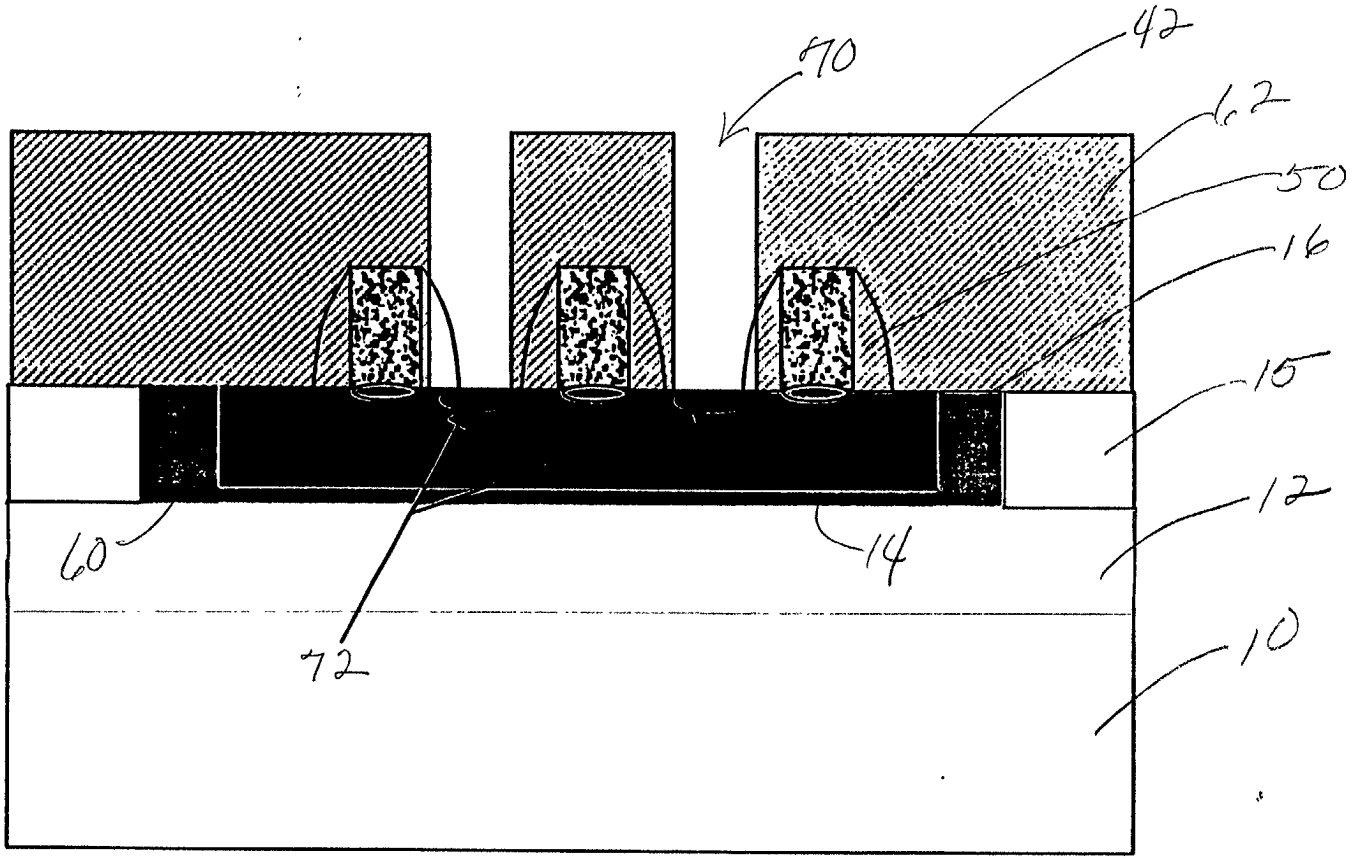


Figure 18

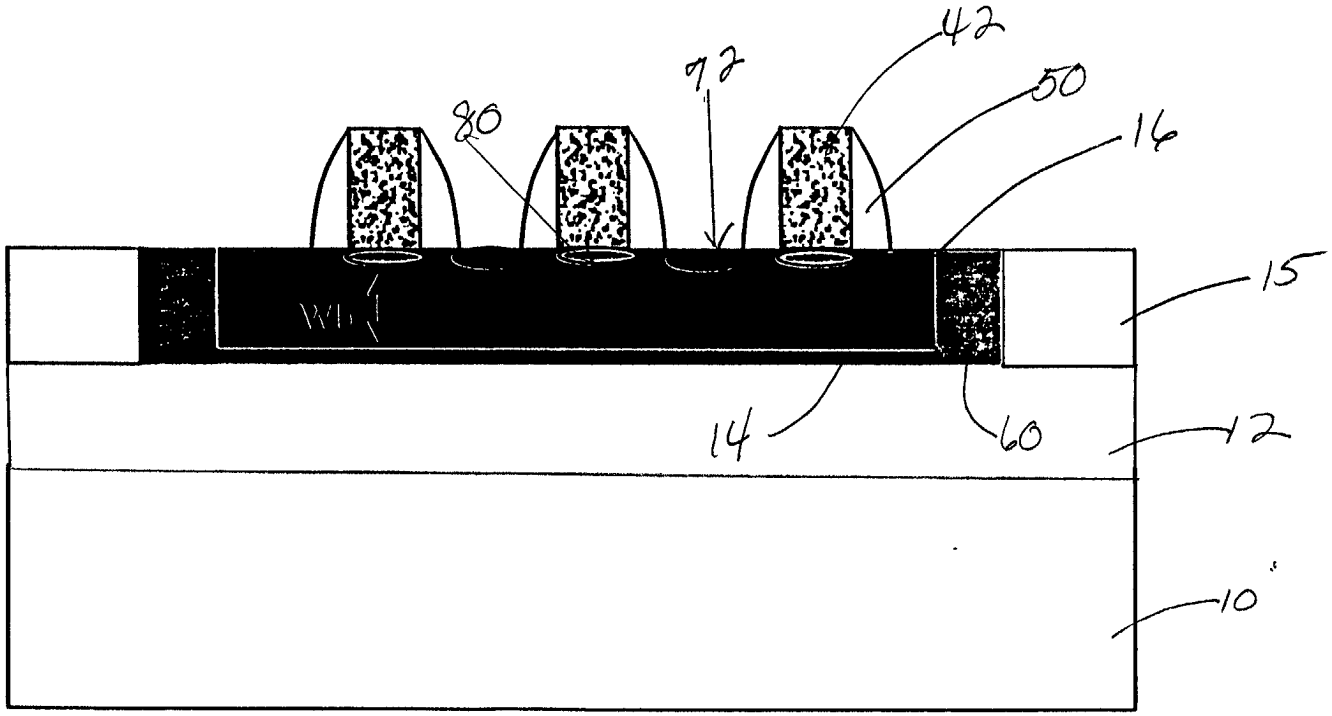
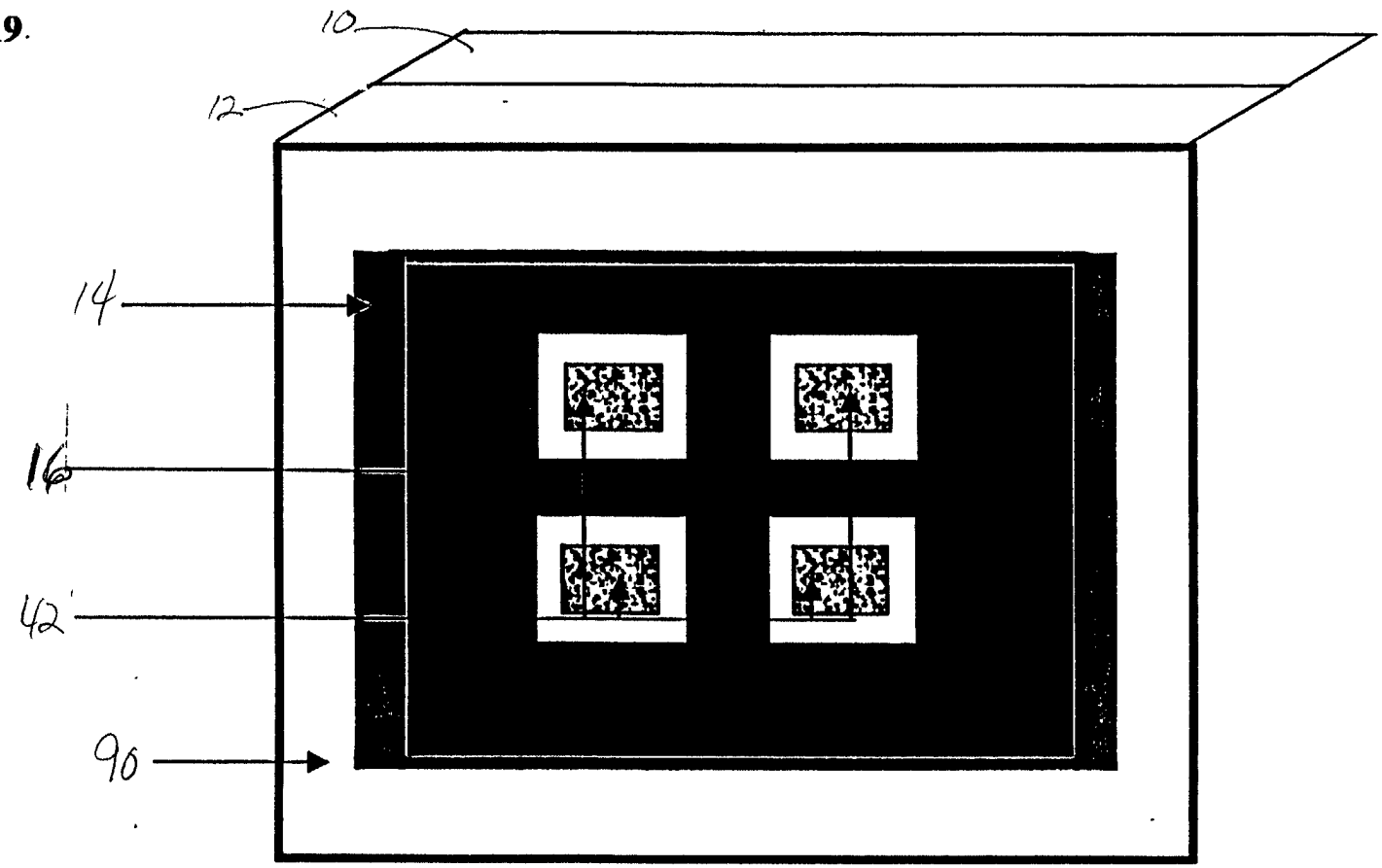


Figure 19.



Collector Doping Profile

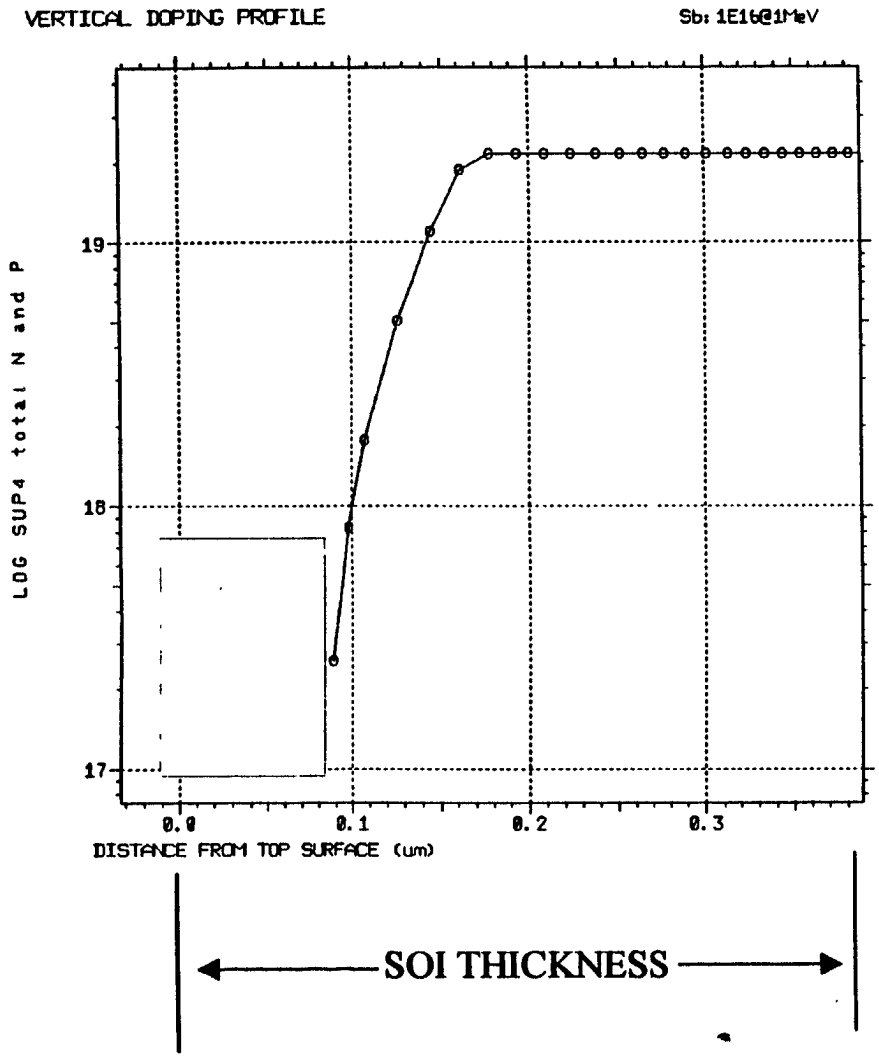


Figure 20A

D.C. Beta vs. Vbe

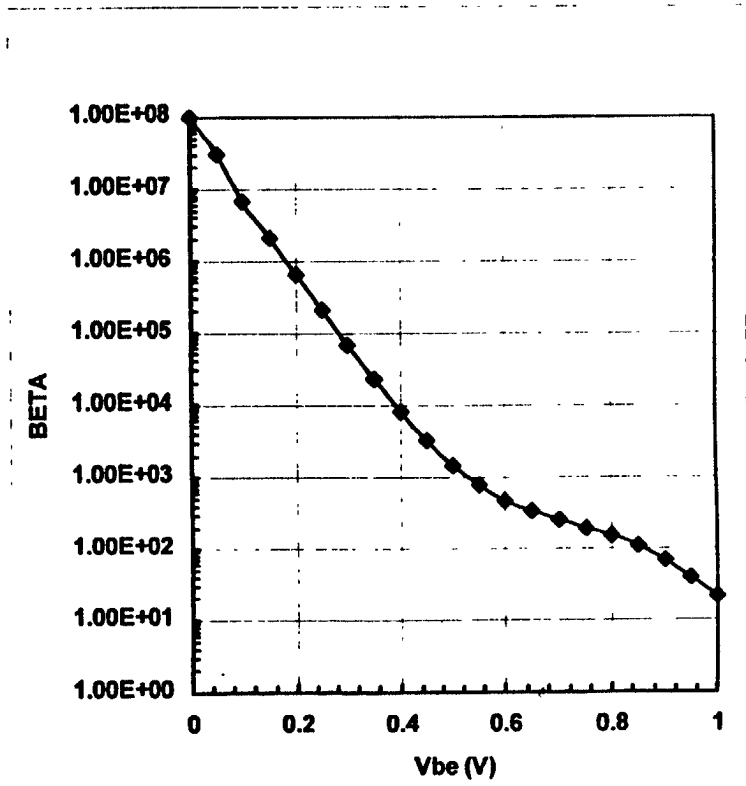


Figure 20B

IBM Docket No.BUR9-2000-0016-US1
EXPRESS LABEL # EL046033892US

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

the specification of which:
(check one)

- ■ is attached hereto.
- □ was filed on _____, as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Mark F. Chadurjian (Reg. No. 30,739), Richard M. Kotulak (Reg. No. 27,712), James M. Leas (Reg. No. 34,372), William D. Sabo (Reg. No. 27,465), Eugene I. Shkurko (Reg. No. 36,678), Robert A. Walsh (Reg. No. 26,516), Howard J. Walter, Jr. (Reg. No. 24,832), Richard A. Henkler (Reg. No. 39,220), Christopher A. Hughes (Reg No. 26,914), Edward A. Pennington (Reg No. 32,588), John E. Hoel (Reg No. 26,279), Joseph C. Redmond, Jr. (Reg No. 18,753), Sean M. McGinn (Reg. No. 34, 386), and Frederick W. Gibb, III (Reg. No. 37,629).

Send all correspondence to: McGinn & Gibb, P.C., 8321 Old Courthouse Road, Suite 200, Vienna, Virginia 22182, Customer No. 21254

Telephone calls should be directed to McGinn & Gibb, P.C. at (703) 761-4100.

(1) Inventor: Ramachandra Divakaruni

Signature: Ramachandra Divakaruni Date: Nov. 17, 00

R.D. Residence: ~~219 Berleman Drive, Middletown, New York 10940~~ 131B Heritage Hills, Somers, New York 10
Citizenship: United States of America
Post Office Address: Same as Residence

IBM Docket No.BUR9-2000-0016-US1
EXPRESS LABEL # EL046033892US

(2) Inventor: Russell J. Houghton

Signature: ____________________ Date: ____________
Residence: 310 Old Stage Road, Essex Junction, VT 05452
Citizenship: United States of America
Post Office Address: Same as Residence

(3) Inventor: Jack A. Mandelman

Signature: Jack A. Mandelman Date: 11-17-00
Residence: 5 Jamie Lane, Stormville, New York 12582
Citizenship: United States of America
Post Office Address: Same as Residence

(4) Inventor: Wilbur D. Pricer

Signature: ____________________ Date: ____________
Residence: 5524 Spear Street, Charlotte, VT 05445
Citizenship: United States of America
Post Office Address: Same as Residence

(5) Inventor: William R. Tonti

Signature: ____________________ Date: ____________
Residence: 4 Bluestem Road, Essex Junction, VT 05452
Citizenship: United States of America
Post Office Address: Same as Residence

(2) Inventor: Russell J. Houghton

Signature: Russell J. Houghton Date: 11/21/00
Residence: 310 Old Stage Road, Essex Junction, VT 05452
Citizenship: United States of America
Post Office Address: Same as Residence

(3) Inventor: Jack A. Mandelman

Signature: _____ Date: _____
Residence: 5 Jamie Lane, Stormville, New York 12582
Citizenship: United States of America
Post Office Address: Same as Residence

(4) Inventor: Wilbur D. Pricer

Signature: _____ Date: _____
Residence: 5524 Spear Street, Charlotte, VT 05445
Citizenship: United States of America
Post Office Address: Same as Residence

(5) Inventor: William R. Tonti

Signature: William R. Tonti Date: 11/20/2000
Residence: 4 Bluestem Road, Essex Junction, VT 05452
Citizenship: United States of America
Post Office Address: Same as Residence

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Signature: _____ Date: _____
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Citizenship: United States of America
Post Office Address: Same as Residence

(4) Inventor: Wilbur D. Pricer

Signature: _____ Date: 11/21/2000
Residence: 5524 Spear Street, Charlotte, VT 05445
Citizenship: United States of America
Post Office Address: Same as Residence

(5) Inventor: William R. Tonti

Signature: _____ Date: 11/20/2000
Residence: 4 Bluestem Road, Essex Junction, VT 05452
Citizenship: United States of America
Post Office Address: Same as Residence